



Dkt. 2271/71525

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application of: Katsuhiko AISU

Serial No.: 10/763,343

Date Filed: January 23, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND AMPLIFIER FOR  
SUPPRESSING POP SOUND WHILE MINIMIZING VOLTAGE TRANSITION  
SETTLING TIME

Conf. No.: 2287

Class-Subclass: 330-151000

**Issue Fee Due Date: April 24, 2008**

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**APPLICANT'S COMMENTS ON  
EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE**

Sir:

Applicant appreciates the Examiner's Statement of the Reasons for Allowance attached to the Notice of Allowability dated January 24, 2008 and submits that the allowed claims recite subject matter which further supports patentability for reasons in addition to those identified in the Reasons for Allowance.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited this date with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Paul Teng  
Reg. No. 40,837  
April 23, 2008  
Date